

PATENT ABSTRACTS OF JAPAN

(11) Publication number : 2004-253610

(43) Date of publication of application : 09.09.2004

(51) Int.CI. H01L 21/66

(21) Application number : 2003-042352 (71) Applicant : MATSUSHITA ELECTRIC IND CO LTD

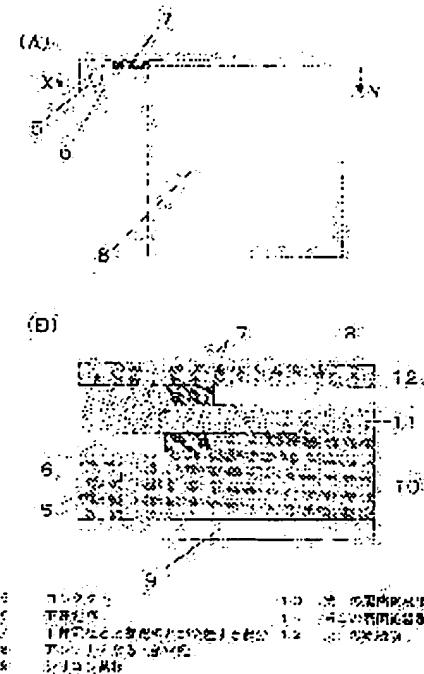
(22) Date of filing : 20.02.2003 (72) Inventor : NARITA KENJI
YAMAGUCHI MINEO

(54) SEMICONDUCTOR DEVICE FOR EVALUATING CHARGEUP DAMAGE AND EVALUATION METHOD THEREOF

(57) Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device for evaluating a chargeup damage capable of detecting the chargeup damage due to static electricity and an evaluation method thereof.

SOLUTION: The semiconductor device for evaluating the chargeup damage comprises a silicon substrate 9, a first isolation film 10 formed on the silicon substrate 9, a first conductor layer 6 connected to the silicon substrate 9 formed on the first isolation film 10, a second isolation film 11 formed on the first conductor layer 6, a second conductor layer 8 acting like an antenna formed on the second isolation film 11, and a third isolation film 12 formed on the second conductor layer 8.



LEGAL STATUS

[Date of request for examination] 12.07.2004

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than

the examiner's decision of rejection or
application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's
decision of rejection]

[Date of requesting appeal against examiner's
decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office

*** NOTICES ***

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1]

A substrate, the first insulator layer formed on this substrate, and the first conductive layer which was formed on this first insulator layer and connected to said substrate, The semiconductor device for charge-up damage assessment equipped with the second insulator layer formed on this first conductive layer, the second conductive layer which is formed on this second insulator layer and serves as an antenna, and the third insulator layer formed on this second conductive layer.

[Claim 2]

Said third insulator layer is a semiconductor device for charge-up damage assessment according to claim 1 which is the ingredient which is easy to be charged.

[Claim 3]

Said third insulator layer is a semiconductor device for charge-up damage assessment according to claim 1 or 2 which has irregularity.

[Claim 4]

Claim 1 which forms the geometrical pattern in the third insulator layer of the upper part of the second conductive layer at least, the semiconductor device for charge-up damage assessment according to claim 2 or 3.

[Claim 5]

Claim 1 whose top face of the third insulator layer is a slit configuration with many parallel slits, claim 2, the semiconductor device for charge-up damage assessment according to claim 3 or 4.

[Claim 6]

Claim 1 which formed many slits in the upper part of the third insulator layer at the radiation configuration, claim 2, the semiconductor device for charge-up damage assessment according to claim 3 or 4.

[Claim 7]

Claim 1 which formed the slit in the upper part of the third insulator layer spirally, claim 2, the semiconductor device for charge-up damage assessment according to claim 3 or 4.

[Claim 8]

The semiconductor device for charge-up damage damage assessment according to claim 1 or 2 with the large ratio of the area of the capacitor part formed by the area, the first conductive layer, and the second conductive layer of the antenna section connected to the second conductive layer.

[Claim 9]

Claim 1 with the large ratio of the thickness of the first insulator layer to the thickness of the second insulator layer, the semiconductor device for charge-up damage assessment according to claim 2 or 8.

[Claim 10]

The charge-up damage assessment approach characterized by computing a defective incidence rate from the number of detection of the defect which inspected claim 1 by which the charge up was carried out with static electricity in the semi-conductor production process, claim 2, claim 3, claim 4, claim 5, claim 6, claim 7, and the semiconductor device for charge-up damage assessment according to claim 8 or 9 with optical defective test equipment, and was generated in the static electricity reason.

[Claim 11]

The semiconductor device for charge-up damage assessment according to claim 5 is inspected with optical defective test equipment. It is the charge-up damage assessment approach which computes a defective incidence rate from the number of detection of the defect generated in the static electricity reason. In case the semiconductor fabrication machines and equipment for charge-up damage assessment are pulled up from a penetrant remover at the washing process in a semi-conductor production process, when pulling up in the parallel direction to said slit of the third insulator layer upper part, The charge-up damage assessment approach which dissociates and is characterized by inspecting each semiconductor fabrication machines and equipment for charge-up damage assessment which pulled up by carrying out with said optical defective test equipment when pulling up in the vertical direction to said slit.

[Translation done.]

*** NOTICES ***

JPO and NCIP are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]**[0001]****[Field of the Invention]**

This invention relates to the semiconductor device for charge-up damage assessment in a semiconductor device production process, and its assessment approach.

[0002]**[Description of the Prior Art]**

Thin-film-izing of gate oxide, such as an MOS transistor, and detailed-ization of wiring are progressing with detailed-izing of a component, and high integration. Therefore, the damage prevention to the oxide film by the charge up in a semi-conductor manufacture process is becoming still more important. Since the charge-up damage of the thin oxide film in the dry etching process by ion beam exposure processes and plasma, such as an ion implantation, was regarded as questionable until now, the MOS (Metal Oxide Semiconductor) capacitor with an antenna as shown by drawing 11 was performing charge-up damage assessment (for example, patent reference 1 reference).

[0003]

In drawing 11, the polish recon film with which the thin film gate oxide from which 101 becomes a silicon substrate and 102 becomes a capacitor field, and 103 become an isolation oxide film, and 104 becomes an antenna electrode is shown. The structure of an MOS capacitor with an antenna formed the isolation oxide film 103 on the silicon substrate 101, and deposited thin film gate oxide 102 after that, and has deposited the polish recon film 104 on the whole surface. the capacitor which generally had antenna ratio:A (A= antenna electrode surface product / capacitor area) to one to 106 times in the MOS capacitor with an antenna -- a logarithm -- it has more than one by the ratio.

[0004]

The assessment approach of the charge-up damage in this MOS capacitor with an antenna processes an ion implantation etc. to this MOS capacitor with an antenna, gives electrical stress by impressing an electrical potential difference to the insulator layer of an MOS capacitor after that, measures the electrical potential difference when coming to carry out dielectric breakdown of the insulator layer, and performs it by computing the rate of failure (destruction of gate oxide) of a capacitor by considering that the chip below a certain threshold voltage (for example, 8 MV/cm) is a defect part. Process conditions are set up so that this MOS capacitor with an antenna may not be destroyed.

[0005]**[Patent reference 1]**

JP,8-203971,A (the two - 3rd page)

[0006]**[Problem(s) to be Solved by the Invention]**

However, in the above-mentioned conventional MOS capacitor for charge-up damage assessment with an antenna, to the damage to the gate oxide 102 in direct electrification of the charge by the ion implantation, plasma etching, an electron ray, etc., although sensibility was high, to static electricity which is generated in friction etc., it had the problem that sensibility was low. In an ion implantation, big electric field are impressed to an antenna electrode. When the impressed electric-field distribution is uneven, a current passes gate oxide 102 by the impressed electric field. In order that the charge of a large quantity may pass gate oxide 102 at this time, destruction of gate oxide 102 arises.

[0007]

Although the electric field impressed to an antenna electrode on the other hand by static electricity generated in friction between insulating materials etc. are large, since the amount of charges is ultralow volume, the flow (current) of a charge to the extent that gate oxide 102 is destroyed is not produced. For this reason, sensibility is low to the charge-up damage according to static electricity with the MOS capacitor with an antenna by the conventional technique. This invention solves the above-mentioned conventional trouble, and it aims at offering the semiconductor device for charge-up damage assessment which can detect the charge-up damage by static electricity, and its assessment approach.

[0008]

[Means for Solving the Problem]

The semiconductor device for claim 1 written charge-up damage assessment A substrate, the first insulator layer formed on this substrate, and the first conductive layer which was formed on this first insulator layer and connected to said substrate, It has the second insulator layer formed on this first conductive layer, the second conductive layer which is formed on this second insulator layer and serves as an antenna, and the third insulator layer formed on this second conductive layer.

[0009]

The first conductive layer which according to the semiconductor device for claim 1 written charge-up damage assessment the best conductive layer is covered by the insulator layer, and has a conductive layer more than a bilayer at least, and is connected to the substrate, Since it has the first insulator layer between the second conductive layer connected to the large area pattern used as an antenna, and a silicon substrate and the first conductive layer and has the second insulator layer between the first conductive layer and the second conductive layer, it is high sensitivity to the charge up by static electricity. Namely, the electrostatic energy by the charge is stored in the second conductive layer lower part used as an antenna by static electricity generated by processing by the production process. Since the electrostatic energy accumulated by degrading the insulator layer between the first conductive layer and the second conductive layer by impression of the high electric field by static electricity is emitted and physical destruction of the insulator layer between the first conductive layer and the second conductive layer occurs, The charge-up damage of the static electricity reason is quantitatively detectable with sufficient sensibility.

[0010]

The semiconductor device for charge-up damage assessment according to claim 2 is an ingredient with which said third insulator layer tends to be charged in claim 1.

[0011]

According to the semiconductor device for claim 2 written charge-up damage assessment, high sensibility besides the same effectiveness as claim 1 is expectable.

[0012]

In claim 1 or claim 2, as for the semiconductor device for charge-up damage assessment according to claim 3, said third insulator layer has irregularity.

[0013]

According to the semiconductor device for claim 2 written charge-up damage assessment, it becomes easy to carry out the charge up of everything but the same effectiveness as claim 1.

[0014]

The semiconductor device for charge-up damage assessment according to claim 4 forms the geometrical pattern in the third insulator layer of the upper part of the second conductive layer at least in claim 1, claim 2, or claim 3.

[0015]

According to the semiconductor device for claim 4 written charge-up damage assessment, there is the same effectiveness as claim 1, claim 2, or claim 3.

[0016]

The semiconductor device for charge-up damage assessment according to claim 5 is a slit configuration in which many parallel slits have the top face of the third insulator layer in claim 1, claim 2, claim 3, or claim 4.

[0017]

According to the semiconductor device for claim 5 written charge-up damage assessment, there is the same effectiveness as claim 1, claim 2, claim 3, or claim 4.

[0018]

The semiconductor device for charge-up damage assessment according to claim 6 forms many slits in the upper part of the third insulator layer in claim 1, claim 2, claim 3, or claim 4 at a radiation configuration.

[0019]

According to the semiconductor device for claim 6 written charge-up damage assessment, there is the same effectiveness as claim 1, claim 2, claim 3, or claim 4.

[0020]

The semiconductor device for claim 7 written charge-up damage assessment forms a slit in the upper part of the third insulator layer spirally in claim 1, claim 2, claim 3, or claim 4.

[0021]

According to the semiconductor device for claim 7 written charge-up damage assessment, there is the same effectiveness as claim 1, claim 2, claim 3, or claim 4.

[0022]

The semiconductor device for charge-up damage assessment according to claim 8 has the large ratio of the area of the capacitor part formed by the area, the first conductive layer, and the second conductive layer of the antenna section connected to the second conductive layer in claim 1 or claim 2.

[0023]

According to the semiconductor device for claim 8 written charge-up damage assessment, it is high sensitivity to the charge up by static electricity besides the same effectiveness as claim 1 or claim 2.

[0024]

The semiconductor device for charge-up damage assessment according to claim 9 has the large ratio of the thickness of the first insulator layer to the thickness of the second insulator layer in claim 1, claim 2, or claim 8.

[0025]

According to the semiconductor device for claim 9 written charge-up damage assessment, the applied voltage by static electricity besides the same effectiveness as claim 1, claim 2, or claim 8 becomes large.

[0026]

The charge-up damage assessment approach according to claim 10 is characterized by computing a defective incidence rate from the number of detection of the defect which inspected claim 1 by which the charge up was carried out with static electricity in the semi-

conductor production process, claim 2, claim 3, claim 4, claim 5, claim 6, claim 7, and the semiconductor device for charge-up damage assessment according to claim 8 or 9 with optical defective test equipment, and was generated in the static electricity reason.

[0027]

According to the claim 10 written charge-up damage assessment approach, the charge-up damage of the static electricity reason can be quantitatively evaluated with sufficient sensibility by detecting the physical destructive part of the semiconductor device for assessment high-sensitivity-ized to static electricity, and computing a defective incidence rate.

[0028]

The charge-up damage assessment approach according to claim 11 The semiconductor device for charge-up damage assessment according to claim 5 is inspected with optical defective test equipment. It is the charge-up damage assessment approach which computes a defective incidence rate from the number of detection of the defect generated in the static electricity reason. In case the semiconductor fabrication machines and equipment for charge-up damage assessment are pulled up from a penetrant remover at the washing process in a semi-conductor production process, when pulling up in the parallel direction to said slit of the third insulator layer upper part, When pulling up in the vertical direction to said slit, it dissociates and is characterized by inspecting each semiconductor fabrication machines and equipment for charge-up damage assessment which pulled up by carrying out with said optical defective test equipment.

[0029]

According to the claim 11 written charge-up damage assessment approach, to the raising direction, it dissociates in the direction vertical to an parallel direction, and the charge-up damage which depended in the raising direction of a semiconductor device is measured, and is made, and a charge-up damage can be evaluated quantitatively, respectively.

[0030]

[Embodiment of the Invention]

Hereafter, each operation gestalt as the semiconductor device for charge-up damage assessment concerning this invention and its assessment approach is explained, referring to a drawing.

[0031]

(First operation gestalt)

It explains referring to drawing 5 from drawing 1 about the semiconductor device for charge-up damage assessment concerning the first operation gestalt of this invention.

[0032]

Drawing 1 (A) shows the surface structure of the semiconductor device for charge-up damage assessment in the gestalt of this operation (it considers as a testing device henceforth), and drawing 1 (B) shows the X-Y line sectional view of drawing 1 (A). The contact for connecting 5 with the silicon (Si) substrate 9 and the lower electrode 6 electrically, the up electrode which forms the large area pattern with which 8 becomes the antenna which accumulates a charge, the part which, as for 7, the lower electrode 6 and the up electrode 8 intersect, the interlayer insulation film which deposited 10 on the silicon substrate 9, the interlayer insulation film which deposited 11 on the interlayer insulation film 10, and the interlayer insulation film which deposited 12 on the interlayer insulation film 11 are shown, respectively. An insulator layer 12 uses the ingredient, for example, the plasma TEOS film and the plasma oxidation film, which is easy to be charged.

[0033]

The part (a detecting element is called below) which detects the charge up by static electricity in this testing device is the interlayer insulation film 11 of the capacitor part (detecting element) 7 with which the lower electrode 6 connected to the up electrode 8 (the antenna section is

called below) used as the antenna which accumulates a charge, and the silicon substrate crosses. It is necessary to enlarge surface ratio of this detecting element 7 and the antenna section 8. For example, the area of a detecting element 7 is constituted so that 10 micrometers of surface ratio of 2, a detecting element, and the antenna section may be set to 1 million. Moreover, insulator layer thickness is thickened compared with the insulator layer thickness used with the MOS capacitor with an antenna of the conventional technique. For example, with the gestalt of this operation, the plasma TEOS (Tetra Ethyl Ortho Silicate) whose specific inductive capacity is 4.2 about the thickness of 400nm and an interlayer insulation film 10 in the thickness of an interlayer insulation film 11 at 400nm and an interlayer insulation film was used. By taking such structure, per unit area, the insulator layer used as the object for detection is destroyed, and static electricity can be detected to high sensitivity also in the amount of electrifications by $3.0 \times 10^{-3} \text{C} / \text{minute static electricity of m}^2$.

[0034]

By considering as the above-mentioned structure below, why electrification by static electricity is detectable with sufficient sensibility is explained.

[0035]

When this testing device front face is charged with static electricity, surface potential rises. Electrostatic energy is accumulated in the capacitor currently formed in the antenna section 8 by lifting of this potential. If it becomes more than constant value with surface potential, the electric field more than isolation voltage will be impressed to the interlayer insulation film 11 of a detecting element 7. By the impression electric field more than the isolation voltage, leakage current occurs in inter-electrode [of a detecting element 7]. Once the flow of a charge is formed of leakage current, the charge accumulated between the up electrodes 8 and interlayer insulation films 11 used as an antenna will flow to a silicon substrate 9 at a stretch. The interlayer insulation film 11 of a detecting element 7 is physically destroyed by rapid bleedoff of this stored charge according to generating of the Joule's heat by the flow of a charge.

[0036]

The equal circuit in drawing 1 B at the time of the maximum front face of a testing device being charged is shown in drawing 2. It is a vacuous dielectric constant ϵ_0 If specific inductive capacity of interlayer insulation films 10 and 11 is set to k the electrostatic capacity of the interlayer insulation film 11 of a part 7 with which the up electrode 8 and the lower electrode 6 cross in drawing 3 -- CA (specific-inductive-capacity: -- k --) Insulator layer thickness : The amount of charges accumulated in the maximum front face of the interlayer insulation film 12 on d_2 , electrode surface product:SA, and amount of stored charge:QX and the up electrode 8 of the part 7 is set to QA. the electrostatic capacity of the insulator layer formed with the interlayer insulation film 10 and interlayer insulation film 11 between the up electrode 8 and the Si substrate 9 -- CB (specific-inductive-capacity: -- k --) Insulator layer thickness : if the electrical potential difference to which the amount of charges accumulated in the maximum front face of the interlayer insulation film 12 on d_1+d_2 , electrode surface product:SB, and amount of stored charge:QY and its up electrode 8 is impressed between QB, the up electrode 8, and the lower electrode 6 is set to V Electrostatic energy E by the charge accumulated between the up electrode 8 and an interlayer insulation film 11, electrostatic capacity CA and CB, and applied voltage V are expressed as follows.

[0037]

[Equation 1]

$$E = \frac{1}{2} \frac{(Q_A + Q_B)^2}{C_A + C_B} = \frac{1}{2} (C_A + C_B) V^2 \quad (1)$$

$$C_A = k \epsilon_0 \frac{S_A}{d_2} \quad (2)$$

$$C_B = k \epsilon_0 \frac{S_B}{d_1 + d_2} \quad (3)$$

$$V = \frac{Q_A + Q_B}{C_A + C_B} \quad (4)$$

[0038]

Generating destruction in the smaller amount of electrifications on the front face of a testing device leads to the charge up being more detectable to high sensitivity to generated static electricity.

[0039]

In order to destroy the interlayer insulation film 11 of the antenna section 8 and a detecting element 7, before leakage current occurs by that the electric field more than isolation voltage occur, and the electric field impressed to the insulator layer destroyed, it is that the electrostatic energy (E) by the charge accumulated between the antenna section 8 and an interlayer insulation film 11 appears in destroying the interlayer insulation film 11 of a detecting element 7 enough, and is accumulated in it a certain degree. Henceforth, let the value (SB/SA) which broke the area of the antenna section 8 by area of a detecting element 7 be an antenna ratio (AR).

[0040]

In order to make high sensitivity generate destruction more to static electricity to generate Area (SB) of the antenna section 8 for making the small amount of electrifications easy to collect is enlarged. In order to enlarge the electrical potential difference which the electrostatic energy (E) by the stored charge is increased, enlarges thickness (d2) of the object insulator layer 11 since stored charge leaks immediately and is not lost, and is impressed to the object insulator layer 11. It is necessary to connect the Si substrate 9 with the lower electrode 6, and to enlarge thickness (d1) of an interlayer insulation film 10.

[0041]

Then, the count result of the correlation of the density of electric charge (C/m²) charged on sufficient testing device front face to destroy a detecting element 7 with static electricity to the thickness (d₂:nm) of the interlayer insulation film 11 depending on the value of CA and CB deposited on the interlayer insulation film 10 is shown in drawing 3. The axis of abscissa of drawing 3 shows the density of electric charge (C/m²) to which the axis of ordinate was charged on the testing device front face with static electricity in the thickness (d₂) of an interlayer insulation film 11. It is a big antenna ratio, and drawing 3 shows having reached electrostatic energy sufficient by the lower density of electric charge destroying the interlayer insulation film 11 of a detecting element, so that the thickness of an interlayer insulation film 11 is large.

[0042]

Moreover, the count result of the correlation of the density of electric charge (C/m²) charged on sufficient testing device front face to destroy a detecting element 7 with static electricity to the thickness (d₁:nm) of the interlayer insulation film 10 deposited on the silicon substrate 9 is shown in drawing 4. However, the thickness (d₂) of an interlayer insulation film 11 is fixed to 400nm. The density of electric charge (C/m²) to which the axis of ordinate was charged on the testing device front face with static electricity in the thickness of the interlayer insulation film 10 which deposited the axis of abscissa of drawing 4 on the Si substrate 9 is shown. Drawing 4 shows being a big antenna ratio, and the thickness of an interlayer insulation film 10 being large, therefore having reached such electrostatic energy sufficient by the lower density of electric charge destroying the interlayer insulation film 11 of a detecting element 7 that the ratio of the thickness of the first insulator layer 10 to the thickness of the second insulator layer 11 is large.

[0043]

Moreover, the count result of the correlation of the density of electric charge (C/m²) to the area of the detecting element 7 which influences the value of CA charged on the testing device front face with static electricity is shown in drawing 5. The axis of abscissa of drawing 5 is the area (the numeric value of the axis of abscissa in drawing, 1.00E-08 [for example,], means 1x10⁻⁸) of a detecting element 7. The same is said of the numeric value of the axis of abscissa of drawing 6 and drawing 7. The axis of ordinate shows the density of electric charge (C/m²) charged on the testing device front face with static electricity. It is a big antenna ratio, and drawing 5 shows having reached electrostatic energy sufficient by the lower density of electric charge destroying the interlayer insulation film 11 of a detecting element, so that the area of a detecting element is large.

[0044]

In order for a testing device to be destroyed more by high sensitivity from the above result to electrification of static electricity, it becomes possible by making or more [10-micrometer] into two area of the part 7 with which an antenna ratio is made or more into 100000, and thickness of interlayer insulation films 10 and 11 is made large to 400nm or more and which the up electrode 8 which is a detecting element, and the lower electrode 6 intersect. By fulfilling these conditions, rather than the conventional MOS capacitor for charge-up damage assessment with an antenna, sensibility becomes high to electrification by static electricity, and a testing device tends to detect the charge up.

[0045]

Next, the charge-up damage assessment approach concerning the first operation gestalt of this invention is explained.

[0046]

With semiconductor fabrication machines and equipment to perform charge-up damage assessment, the testing device which is high sensitivity is processed to electrification by above-mentioned static electricity. Static electricity occurs by performing processing with the

semiconductor fabrication machines and equipment for [that] assessment, and if the charge beyond the value in a testing device front face is charged, destruction will occur in the charge-up detecting element of this testing device.

[0047]

The testing device which the destruction generated is put in in optical defective test equipment, in a chip, it divides for every antenna ratio and an inspecting region is set up. if for example, an antenna ratio is three kinds of 1 and 10,100 -- a test 1 -- an antenna ratio sets up an inspecting region only for the field of 1 so that only the field of the antenna ratio 10 may inspect only the field of the antenna ratio 100 in a test 3 by the test 2. Moreover, sensitivity settling is carried out so that only destruction of a charge-up detecting element may be detected and foreign matters, such as particle, may not be detected. Only the number of defects by destruction of a charge-up detecting element is detectable for every antenna ratio with these setting out. The defective incidence rate of a testing device is computable for every antenna ratio after these setting out from the number of defects detected by carrying out defective inspection.

Below, the example which evaluated the charge-up damage by static electricity by structure of the first operation gestalt is shown.

[0048]

A formula (1) shows that the electrostatic energy by the charge accumulated increases along with the increment in the amount of charges accumulated. It becomes possible to generate a charge-up damage with sufficient sensibility by enlarging area of the up electrode 8 used as an antenna, and making the amount of charges accumulated increase from this. The membrane type of the interlayer insulation film 11 deposited here on the interlayer insulation film 10 deposited on the silicon substrate 9, and the interlayer insulation film 10 The plasma TEOS film (specific inductive capacity: 4.2), So that area of the part 7 which the up electrode 8 which are 400nm and a detecting element, and the lower electrode 6 intersect in thickness may be made into constant value (=10micrometer²) and an antenna ratio may be set to 1, 10, 100, 1000, 10000, 100000, and 1 million It experimented with a testing device which has arranged a total (A) of seven kinds of drawing 1 in 1 chip. The testing device was processed with the semiconductor fabrication machines and equipment for charge-up assessment. Optical defective test equipment detected the defect generated by the charge up of static electricity, and the defective incidence rate was computed from the number of detection. The result is shown in drawing 6 . In drawing 6 , an axis of abscissa shows the antenna ratio of a testing device, and the axis of ordinate shows the defective incidence rate (%). Drawing 6 shows that the defective incidence rate is also increasing with the increment in an antenna ratio.

Moreover, the correlation of the electrostatic energy and the defective incidence rate by the charge accumulated between the up electrodes 8 of the antenna section and interlayer insulation films 11 for which it asked from the count based on the formula at the time of the antenna ratio 10000 (1), (2), (3), and (4) is shown in drawing 7 . In drawing 7 , the electrostatic energy (J) by the charge accumulated between the up electrodes 8 and interlayer insulation films 11 with which an axis of abscissa serves as an antenna, and an axis of ordinate show the defective incidence rate (%). From drawing 7 , the defective incidence rate went up [electrostatic energy] rapidly more than 1.0microJ.

As mentioned above, according to this operation gestalt, an antenna ratio can be enlarged and detecting destruction by the charge up with optical defective test equipment can estimate the charge-up damage by static electricity quantitatively using the testing device which raised the detection sensitivity of the charge up.

[0049]

(Second operation gestalt)

It explains referring to drawing 10 from drawing 8 about the semiconductor device for charge-up assessment concerning the second operation gestalt of this invention. Drawing 8 shows

structural drawing of the second semiconductor device for charge-up assessment of this invention. Drawing 8 (A) shows the surface structure of the testing device in the gestalt of the second operation, and drawing 8 R> 8 (B) shows the X-Y line sectional view of drawing 8 (A). [0050]

The contact for connecting 5 with a silicon substrate 9 and the lower electrode 6 electrically, The up electrode with which 8 becomes the antenna which accumulates a charge, the part which, as for 7, the lower electrode 6 and the up electrode 8 intersect, The interlayer insulation film which deposited 10 on the silicon substrate 9, the interlayer insulation film which deposited 11 on the interlayer insulation film 10, and 13 show the topmost part insulator layer (for example, a pitch: 1 micrometer) processed in the shape of [which was deposited on the interlayer insulation film 11 / which has many parallel slits, for example] a slit, respectively. By using this structure, a directive charge-up damage is detectable.

(Third operation gestalt)

Hereafter, the example which measured the charge up is shown using the semiconductor device for charge-up assessment of the second operation gestalt. The assessment approach is the same as that of the gestalt of the first operation.

Drawing 9 shows the approach in the multi-tub type soak cleaning equipment by ultrapure water to pull up the semiconductor device P for charge-up assessment of this invention as a penetrant remover. By the case where the raising direction and the direction of a slit 14 are made parallel, drawing 9 (A) shows the case where drawing 9 (B) makes vertical the raising direction and the direction of a slit 14. Drawing 10 is drawing in which pulling up about each direction and showing the relation between a rate (mm/s) and the rate of destruction of the semiconductor device for charge-up assessment of this invention here. In drawing 10, an axis of abscissa expresses the raising rate (mm/s) of a semiconductor device, and the axis of ordinate expresses the defective incidence rate (%). Here, to the quartz tub 15, ultrapure water 16 (resistivity: 18.0 M omega-cm) is filled. To this ultrapure water 16, it was immersed for 2 minutes and the semiconductor device for charge-up assessment of this invention was pulled up by the lifter.

[0051]

If a raising rate increases from drawing 10 also in which [the case of drawing 9 (A), and in the case of drawing 9 (B)], the defective incidence rate will also increase. This is considered for the workload by frictional force F' which works between a substrate and the ultrapure water 16 in the quartz tub 15 to per unit time amount to increase as a raising rate increases. Moreover, the touch area of ultrapure water 16 and a substrate (P) also becomes [the direction in case the raising direction of drawing 9 (A) and the direction of a slit 14 are parallel] large. Moreover, since ultrapure water 16 is easy to flow between slits 14 in response to gravity acceleration, the workload by frictional force F' which the direction in the case of drawing (A) commits between ultrapure water becomes large rather than the case of drawing 9 (B) as a result.

[0052]

Therefore, static electricity will occur by the friction, the amount of charges accumulated in the topmost part insulator layer 13 processed in the shape of a slit will also increase along with the increment in a raising rate, the electrical potential difference V concerning the third insulator layer 13 will increase proportionally, and the rate of destruction of a semiconductor device will rise.

[0053]

As mentioned above, according to this operation gestalt, the front face of the topmost part insulator layer 13 of the semiconductor device of this invention can be processed into the raising direction and parallel in the shape of a slit, and promoting the touch area of ultrapure water 16 and a substrate (P) and the drop rate of ultrapure water 16 can estimate a charge-up damage quantitatively to the ultrapure water 16 which is an insulator, and static electricity

produced in friction between the topmost part insulator layers 13 which processed it on the slit.

[0054]

With this operation gestalt, it has the description which dissociates in the direction vertical to an parallel direction, and can measure the charge-up damage which depended in the raising direction of a semiconductor device to the raising direction.

[0055]

In addition, by processing spirally the configuration of the slit of the topmost part insulator layer 13, the touch area of the ultrapure water and the topmost part insulator layer 13 in a rotating type sheet washing station which were breathed out becomes large, it becomes easy to generate static electricity, and sensibility goes up.

[0056]

Moreover, the third insulator layer 13 may have irregularity and this invention may form a geometrical pattern in the third insulator layer 13 of the upper part of the second conductive layer 8 at least. Furthermore, many slits may be formed in the upper part of the third insulator layer 13 at a radiation configuration.

[0057]

[Effect of the Invention]

According to the semiconductor device for claim 1 written charge-up damage assessment, with static electricity generated by processing by the production process By storing the electrostatic energy by the charge in the second conductive layer lower part used as an antenna, and degrading the insulator layer between the first conductive layer and the second conductive layer by impression of the high electric field by static electricity Since the accumulated electrostatic energy is emitted and physical destruction of the insulator layer between the first conductive layer and the second conductive layer occurs, the charge-up damage of the static electricity reason is quantitatively detectable with sufficient sensibility.

[0058]

According to the semiconductor device for claim 2 written charge-up damage assessment, high sensibility besides the same effectiveness as claim 1 is expectable.

[0059]

According to the semiconductor device for claim 3 written charge-up damage assessment, it becomes easy to carry out the charge up of everything but the same effectiveness as claim 1.

[0060]

According to the semiconductor device for claim 4 written charge-up damage assessment, there is the same effectiveness as claim 1, claim 2, or claim 3.

[0061]

According to the semiconductor device for claim 5 written charge-up damage assessment, there is the same effectiveness as claim 1, claim 2, claim 3, or claim 4.

[0062]

According to the semiconductor device for claim 6 and claim 7 written charge-up damage assessment, there is the same effectiveness as claim 1, claim 2, claim 3, or claim 4.

[0063]

According to the semiconductor device for claim 8 written charge-up damage assessment, it is high sensitivity to the charge up by static electricity besides the same effectiveness as claim 1 or claim 2.

[0064]

According to the semiconductor device for claim 9 written charge-up damage assessment, the applied voltage by static electricity besides the same effectiveness as claim 1, claim 2, or claim 8 becomes large.

[0065]

According to the claim 10 written charge-up damage assessment approach, the charge-up damage of the static electricity reason can be quantitatively evaluated with sufficient sensibility by detecting the physical destructive part of the semiconductor device for assessment high-sensitivity-ized to static electricity, and computing a defective incidence rate.

[0066]

According to the claim 11 written charge-up damage assessment approach, to the raising direction, it dissociates in the direction vertical to an parallel direction, and the charge-up damage which depended in the raising direction of a semiconductor device is measured, and is made, and a charge-up damage can be evaluated quantitatively, respectively.

[Brief Description of the Drawings]

[Drawing 1] Surface drawing in which (A) shows the surface structure of the semiconductor device for charge-up damage assessment of this invention, and (B) are drawings showing the cross section of the X-Y line of (A).

[Drawing 2] It is the explanatory view showing the equal circuit in drawing 1 (B) when the maximum front face of the semiconductor device for charge-up damage assessment of this invention is charged with semiconductor fabrication machines and equipment.

[Drawing 3] In a different antenna ratio, it is drawing to the thickness (nm) of the interlayer insulation film 11 deposited on the interlayer insulation film 10 showing the correlation of the density of electric charge charged on the testing device front face with static electricity.

[Drawing 4] In a different antenna ratio, it is drawing showing correlation drawing of the density of electric charge to the thickness (nm) of an interlayer insulation film 10 charged on the testing device front face with static electricity.

[Drawing 5] In a different antenna ratio, it is drawing showing correlation drawing of the density of electric charge to the area of the part 7 which the lower electrode 6 connected with the up electrode 8 and Si substrate intersects charged on the testing device front face with static electricity.

[Drawing 6] It is drawing showing the result of the defective incidence rate computed from the number of detection of the defect by the optical defective test equipment of the semiconductor device for charge-up assessment of this invention showing the correlation over an antenna ratio.

[Drawing 7] It is drawing showing the correlation of the electrostatic energy (J) and the defective incidence rate by the charge accumulated between the up electrodes 8 and interlayer insulation films 11 used as an antenna.

[Drawing 8] Surface drawing in which (A) shows the surface structure of the second semiconductor device for charge-up damage assessment of this invention, and (B) are drawings showing the cross-section structure of the X-Y line of (A).

[Drawing 9] In the approach of pulling up (A) from the tub of the semiconductor device for charge-up assessment in the gestalt of operation of the third of this invention, an explanatory view when the raising direction and the direction of a slit are parallel, and (B) are explanatory views when the raising direction and the direction of a slit are vertical.

[Drawing 10] It is related drawing showing the relation of the raising rate from the washing station of the defective incidence rate by the charge-up damage of a semiconductor device, and a semiconductor device.

[Drawing 11] It is drawing showing the cross-section structure of the conventional MOS capacitor for charge-up damage assessment with an antenna.

[Description of Notations]

5 Contact

6 Lower Electrode

7 Part Which Lower Electrode and Up Electrode Intersect

8 Up Electrode Used as Antenna

- 9 Silicon Substrate
- 10 First Interlayer Insulation Film
- 11 Second Interlayer Insulation Film
- 12 Third Insulator Layer
- 13 Third Insulator Layer Processed in the shape of a Slit
- 14 Slit
- 15 Quartz Tub
- 16 Ultrapure Water
- 101 Silicon Substrate
- 102 Thin Film Gate Oxide Used as Capacitor Field
- 103 Isolation Oxide Film
- 104 Polish Recon Film Used as Antenna Electrode

[Translation done.]

*** NOTICES ***

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] Surface drawing in which (A) shows the surface structure of the semiconductor device for charge-up damage assessment of this invention, and (B) are drawings showing the cross section of the X-Y line of (A).

[Drawing 2] It is the explanatory view showing the equal circuit in drawing 1 (B) when the maximum front face of the semiconductor device for charge-up damage assessment of this invention is charged with semiconductor fabrication machines and equipment.

[Drawing 3] In a different antenna ratio, it is drawing to the thickness (nm) of the interlayer insulation film 11 deposited on the interlayer insulation film 10 showing the correlation of the density of electric charge charged on the testing device front face with static electricity.

[Drawing 4] In a different antenna ratio, it is drawing showing correlation drawing of the density of electric charge to the thickness (nm) of an interlayer insulation film 10 charged on the testing device front face with static electricity.

[Drawing 5] In a different antenna ratio, it is drawing showing correlation drawing of the density of electric charge to the area of the part 7 which the lower electrode 6 connected with the up electrode 8 and Si substrate intersects charged on the testing device front face with static electricity.

[Drawing 6] It is drawing showing the result of the defective incidence rate computed from the number of detection of the defect by the optical defective test equipment of the semiconductor device for charge-up assessment of this invention showing the correlation over an antenna ratio.

[Drawing 7] It is drawing showing the correlation of the electrostatic energy (J) and the defective incidence rate by the charge accumulated between the up electrodes 8 and interlayer insulation films 11 used as an antenna.

[Drawing 8] Surface drawing in which (A) shows the surface structure of the second semiconductor device for charge-up damage assessment of this invention, and (B) are drawings showing the cross-section structure of the X-Y line of (A).

[Drawing 9] In the approach of pulling up (A) from the tub of the semiconductor device for charge-up assessment in the gestalt of operation of the third of this invention, an explanatory view when the raising direction and the direction of a slit are parallel, and (B) are explanatory views when the raising direction and the direction of a slit are vertical.

[Drawing 10] It is related drawing showing the relation of the raising rate from the washing station of the defective incidence rate by the charge-up damage of a semiconductor device, and a semiconductor device.

[Drawing 11] It is drawing showing the cross-section structure of the conventional MOS capacitor for charge-up damage assessment with an antenna.

[Description of Notations]

5 Contact

- 6 Lower Electrode
- 7 Part Which Lower Electrode and Up Electrode Intersect
- 8 Up Electrode Used as Antenna
- 9 Silicon Substrate
- 10 First Interlayer Insulation Film
- 11 Second Interlayer Insulation Film
- 12 Third Insulator Layer
- 13 Third Insulator Layer Processed in the shape of a Slit
- 14 Slit
- 15 Quartz Tub
- 16 Ultrapure Water
- 101 Silicon Substrate
- 102 Thin Film Gate Oxide Used as Capacitor Field
- 103 Isolation Oxide Film
- 104 Polish Recon Film Used as Antenna Electrode

[Translation done.]

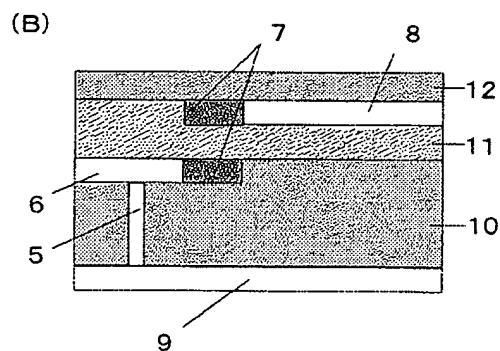
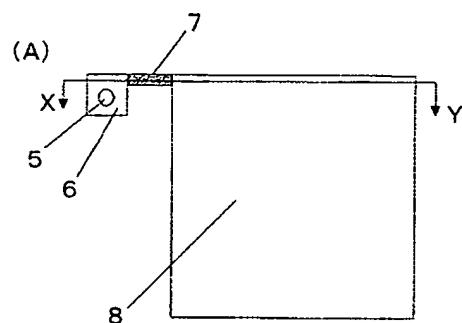
* NOTICES *

JPO and NCIPI are not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer. So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3. In the drawings, any words are not translated.

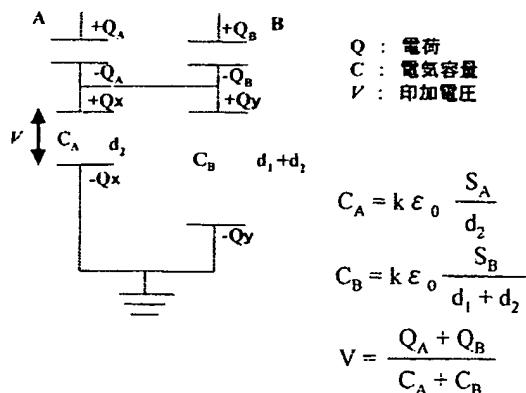
DRAWINGS

[Drawing 1]



5	コンタクト	10	第一の層間絶縁膜
6	下部電極	11	第二の層間絶縁膜
7	下部電極と上部電極とが交差する部分	12	第三の絶縁膜
8	アンテナとなる上部電極		
9	シリコン基板		

[Drawing 2]

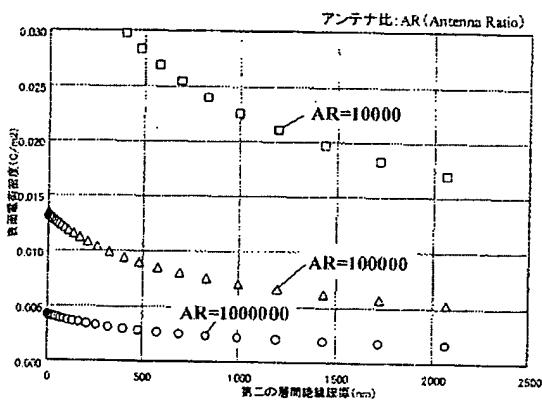


A:上部電極と下部電極が交差する部分
B:上部電極と下部電極が交差しない部分

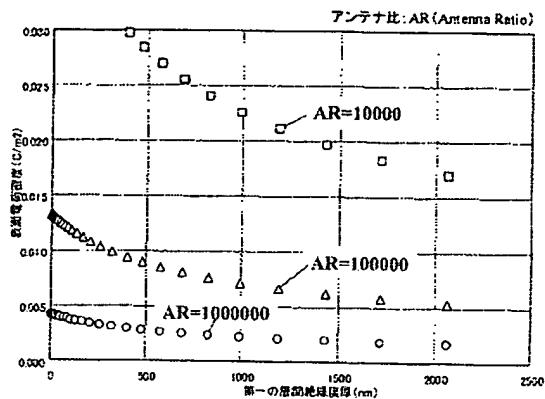
蓄積電荷による静電エネルギー

$$E = \frac{1}{2} \frac{(Q_A + Q_B)^2}{C_A + C_B} = \frac{1}{2} (C_A + C_B) V^2$$

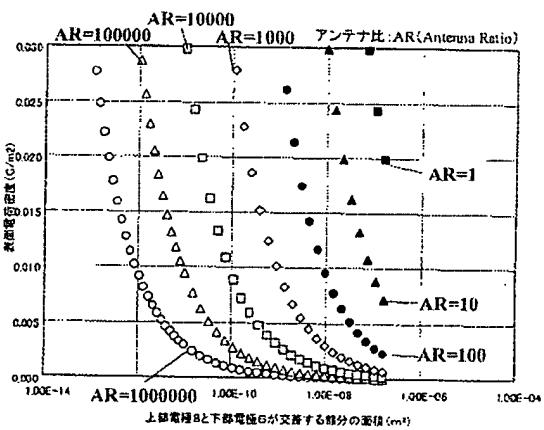
[Drawing 3]



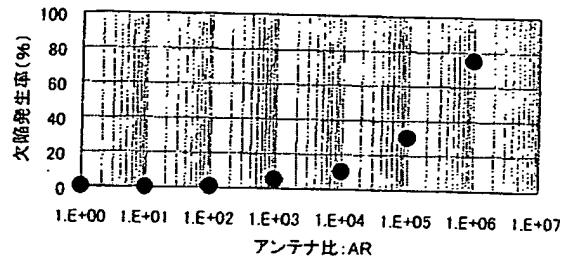
[Drawing 4]



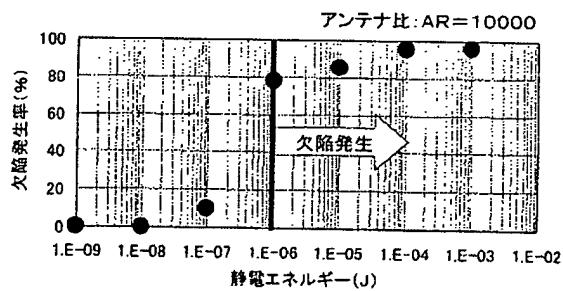
[Drawing 5]



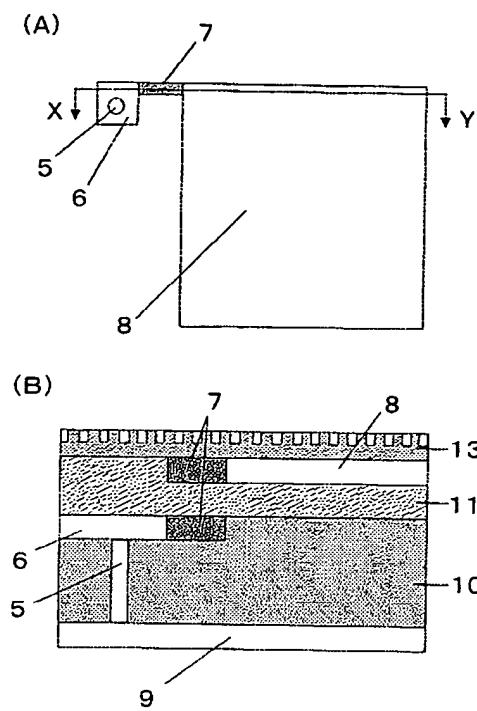
[Drawing 6]



[Drawing 7]

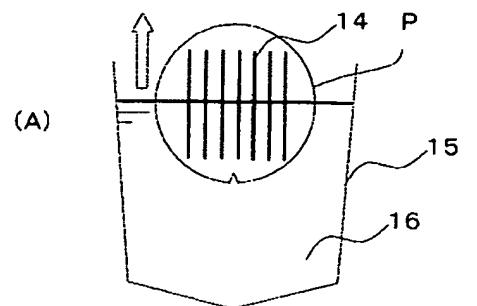


[Drawing 8]

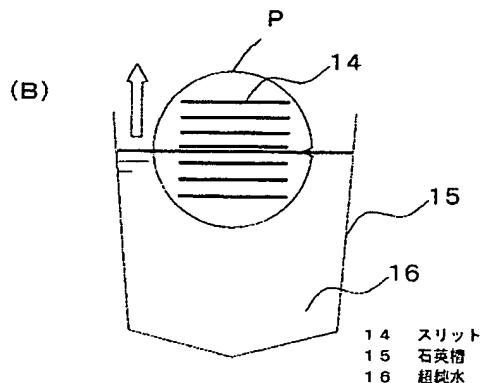


13 スリット状に加工した第三の絶縁膜

[Drawing 9]

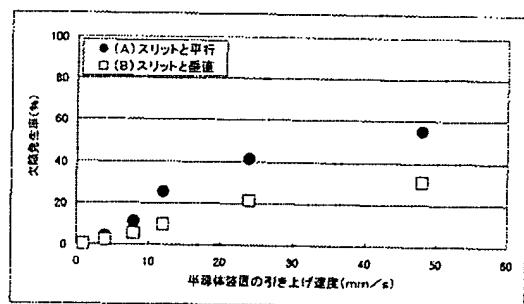


引き上げ方向と平行

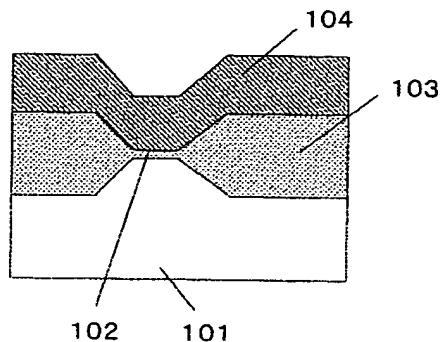


引き上げ方向と垂直

[Drawing 10]



[Drawing 11]



101 シリコン基板
102 キャバシタ領域となる薄膜ゲート酸化膜
103 素子分離酸化膜
104 アンテナ電極となるポリシリコン膜

[Translation done.]